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| KALAM, ABUL | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/801,838 | UEDA, NAOHIRO | |
| | Examiner | Art Unit | |
| | Abul Kalam | 2814 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *29 December 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-10 and 17-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 17-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/10/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. **Claims 1-4, 17 and 22-26** are rejected under 35 U.S.C. 103(a) as being obvious over **Reiner (US 2003/0042499; previously cited)** in view of **Zuniga et al. (US 2002/0000671; previously cited, hereinafter, Zuniga)**.

With respect to **claim 1, Reiner** teaches a semiconductor apparatus **(Fig. 2)** comprising:

a semiconductor substrate **(p-Substrate, Fig. 2, ¶ [0036])**;

a metal wiring layer **(metal 2, Fig. 2, ¶ [0036])** formed over the semiconductor substrate;

a material layer **(see depiction of Fig. 2 below)** formed over the metal wiring layer **(metal 2)** and having a window therein;

a first electrode pad **(4, Fig. 2)** formed over the semiconductor substrate **(p-substrate)**, and exposed through said window for providing contact between said semiconductor apparatus and external circuitry **(Fig. 2, ¶ [0036]: it is implicit that bond pad 4 provides contact between the semiconductor apparatus and external circuitry)**;

a circuit **(2, Fig. 3)** formed over said semiconductor substrate **(p-susbstrate)** in a region under the window in the material layer exposing the first electrode pad **(4, Fig. 2, ¶ [0038])**, said circuit comprising an array of adjacent resistive elements **(23-25, Fig. 3)** formed of a semiconductor material **(¶ [0038]: "polysilicon")**.

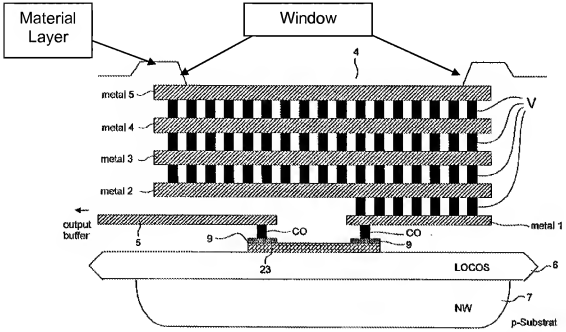


FIG.2

Thus, Reiner teaches all the limitations of the claim with the exception of explicitly disclosing wherein said first electrode pad being formed over said array of resistive elements such that said first electrode pad extends transversely across said array.

However, **Zuniga** discloses an analogous semiconductor apparatus wherein an electrode pad **(514/515, Figs. 5 and 6)** is formed over an array of resistive elements **(passive resistors)** such that said electrode pad **(514/515)** extends transversely across

said array **(¶ [0052], Figs. 5 and 6)**. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to form the electrode pad over Reiner's array of resistive elements, as taught by Zuniga, for the disclosed intended purpose of saving chip space **(¶ [0049])** and protecting the underlying circuit components **(¶ [0053])**.

With respect to **claim 2, Reiner** teaches wherein the resistive elements **(23-25, Fig. 3)** comprise polysilicon **(¶ [0038])**.

With respect to **claim 3, Reiner** teaches wherein the resistive elements include a plurality of resistors connected serially **(Fig. 4)**

With respect to **claim 4, Zuniga** teaches a MOS transistor **(¶ [0050])** formed over the semiconductor substrate **(701, Fig. 5)** wherein the MOS transistor includes a gate electrode **(508)** which comprises polysilicon **(¶ [0050])**.

Regarding **claim 17, Reiner** teaches wherein the resistive elements includes a plurality of doped semiconductor material resistors **(¶ [0026])**.

Regarding **claim 22, Reiner** teaches wherein the first electrode pad **(4, Fig. 2)** is formed on an uppermost metal wiring layer **(metal 5)** of the semiconductor apparatus, and wherein said uppermost metal wiring **(metal 5)** is substantially entirely cover by said material layer **(Fig. 2)**.

Regarding **claim 23, Reiner** teaches a rerouting layer **(metal 1-4)** including a second metal wiring layer **(metal 4)** formed on the material layer and a second electrode pad **(metal 1)**, wherein the first electrode pad **(4)** is configured to provide

contact between the semiconductor apparatus and the external circuitry via the rerouting layer **(metal 1-4)**.

Regarding **claim 24, Reiner** teaches wherein the material layer **(the insulating layer covering metal layers 1-5, Fig. 2)** is a passivation layer **(implicit)**. Furthermore, Zuniga teaches wherein a passivation **(510, Fig. 5)** comprises a silicon nitride film. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to form the passivation layer using silicon nitride, because such a material is preferable for its protective properties.

Regarding **claims 25 and 26,** neither Reiner nor Zuniga teach wherein the metal wiring layer comprises a metal alloy containing silicon of approximately 1 weight percent; and wherein the electrode pad comprises a material substantially equivalent to a material of the metal wiring layer. However, note the specification does not disclose such limitations to be critical nor yield unpredictable results. Furthermore, such a material would have been obvious to one of ordinary skill in the art, at the time of the invention, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

2. **Claims 5 and 6** are rejected under 35 U.S.C. 103(a) as being obvious over **Reiner ('499)** and **Zuniga ('671)**, as applied to claim 1 above, and further in view of **Takasu et al. (US 2002/0145177; previously cited, hereinafter, Takasu)**.

Regarding **claim 5, Reiner** discloses the semiconductor apparatus further comprising an insulating film **(6, Fig. 2)** formed on the semiconductor substrate in a region in a vicinity of the first electrode pad **(metal 1-5)**. However, neither Reiner nor Zuniga disclose a fuse element formed on the insulating film, said fuse element being in electrical contact with said plurality of resistive elements. However, Takasu teaches a semiconductor apparatus including a fuse element **(501, Fig. 1, ¶ [0069])** formed on an insulating film **(102, FIG. 1)**, said fuse element in electrical contact with a plurality of resistive elements **(¶ [0071])**. Therefore, it would have been obvious to one of ordinary skill in the art, at the time of the invention, to incorporate the teachings of Takasu, for the purpose of forming a semiconductor device at a low cost and high performance, which includes an analog IC with high precision **(¶ [0040])**.

Regarding **claim 6, Takasu** teaches wherein the fuse element **(501)** comprises silicon **(¶ [0069])**. Note, regarding the limitation of "polysilicon," such a material for a fuse element is well known and conventional, and thus would have been obvious to one of ordinary skill in the art at the time of the invention.

3. **Claim 7** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Reiner ('499), Zuniga ('671) and Takasu ('177)** as applied to claim 5 above, and further in view of **Matsuzaki et al. (US 2002/0063262, previously cited, hereinafter, Matsuzaki)**.

With respect to **claim 7, Reiner, Zuniga and Takasu** teach all the limitations of the claim, as set forth above in claims 1 and 5, with the exception of disclosing:

a rerouting layer formed in a region above the fuse element; and

an external connection terminal formed on the rerouting layer in a region different from a formation region of the electrode pad.

However, **Matsuzaki** teaches a semiconductor apparatus **(FIG. 3)** wherein a rerouting layer **(148)** is formed in a region above a fuse element **(142; pg. 5: [0093])**; and an external connection terminal **(150)** is formed on the rerouting layer in a region different from a formation region of the electrode pad **(143) (pg. 4: [0080]-[0081])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Matsuzaki, into the semiconductor apparatus, for the disclosed intended purpose of connecting the semiconductor apparatus to an electrode of another chip, thereby forming a multi-chip apparatus **(pg. 4: [0082])**.

4. **Claims 8-10** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Reiner ('499), Zuniga ('671; cited above) and Takasu ('177)** as applied to claim 5 above, and further in view of **Tsuchida (US 6,232,823, previously cited)**.

With respect to **claim 8, Reiner, Zuniga and Takasu** teach the semiconductor apparatus as set forth in claim 5 above, with the exception of disclosing:

wherein the circuit comprises a voltage setting circuit, the resistive elements comprise at least two resistors for producing a split voltage based on an input source power voltage, and the voltage setting circuit changes the split voltage according to a condition of the fuse element.

However, **Tsuchida** teaches voltage setting circuit **(fig. 1)**, in which a resistive elements comprise at least two resistors **(22, 23, 24, 25, 26)** for producing a split voltage based on an input source power voltage **(21)**, and the voltage setting circuit changes the split voltage according to a condition of the fuse element **(27, 28, 29, 30) (col. 7: lns. 7-64)**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Tsuchida, into the semiconductor apparatus, for the disclosed intended purpose of providing a voltage setting circuit, in which the number of choices in the output voltage is increased while suppressing the increase of an area occupied by resistors **(col. 2, lns. 24-27)**.

With respect to **claim 9, Tsuchida** teaches **(fig. 6)** wherein the resistive elements comprise at least two resistors **(22, 23, 24, 25, 26)** for producing a split voltage **(col. 11: lns. 51-55; col. 7: 45-64)** based on an input source power voltage **(53)**, the circuit comprises a reference voltage generator **(51)** for generating a reference voltage **(col. 11: lns. 61-63)** and a voltage detector including a comparator **(52)** for performing a comparison of the split voltage with the reference voltage **(col. 11: lns. 50-67; col. 12, lns. 1-33)**. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Tsuchida, into the semiconductor apparatus, for the reasons stated above in claim 8.

With respect to **claim 10, Tsuchida** further teaches **(fig. 6)** wherein the apparatus further comprises an output driver **(54)** for controlling an output voltage **(55)** based on an input voltage **(53)**, and the comparator **(52)** of the voltage detector outputs

a gate control voltage **("operation voltage")** as a result of the comparison for controlling the output driver **(54)** to control the output voltage **(col. 11, lns. 61-67; col. 12, lns. 1-5)**. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Tsuchida, into the semiconductor apparatus, for the reasons stated above in claim 8.

5. **Claim 18** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Reiner ('499)** and **Zuniga ('671)** as applied to claim 4 above, and further in view of **Kohda et al. (US 5,107,313, previously cited, hereinafter, Kohda)**.

With respect to **claim 18, Reiner and Zuniga** do not disclose wherein the gate electrode has lengthwise ends which are bent in an upward direction over the oxide film.

However, **Khoda** teaches a semiconductor apparatus wherein the gate electrode **(4b)** has lengthwise ends which are bent in an upward direction over an oxide film **(2) (FIG. 10; col. 6, lns. 6-12)**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to incorporate the teaching of Khoda, in order to form the gate electrode with lengthwise ends bent in upward direction over an oxide film, for the disclosed intended purpose of reducing the horizontal spacing between the gates, which thereby reduces the cell area and leads to a higher cell density of memory devices **(col. 6: lns. 21-24)**.

6. **Claims 19 and 20** are rejected under 35 U.S.C. 103(a) as being obvious over **Takasu ('177)** and **Zuniga ('671)** in view of **Reiner ('499)**.

With respect to **claim 19, Takasu** teaches a semiconductor apparatus **(FIG. 1)** comprising:

a semiconductor substrate **(101, ¶ [0044])**;

an oxide film **(102, ¶ [0044])** formed over the semiconductor substrate **(101)**, the oxide film comprising a resistive-element formation region **(410, ¶ [0060])** and fuse element formation region **(510, ¶ [0068])**, the resistive element forming region **(410)** having a circuit comprising an array of strip-shaped resistive elements **(¶ [0061], FIG. 1)** formed of a semiconductor material **(¶ [0061]: "silicon")**;

an insulating layer **(104, ¶ [0062])** formed over the oxide film **(102, FIG. 1)** and having an electrode-pad formation region **(105)**,

wherein the electrode-pad formation region **(105, ¶ [0062])** is formed over the resistive-element formation region **(410, FIG. 1)**, and wherein the electrode-pad formation region has an electrode pad comprising a metal layer **(¶ [0062]: "aluminum")** providing contact between said semiconductor apparatus and external circuitry **(it is implicit that aluminum electrodes 105 provide contact between external circuitry and the semiconductor apparatus)**; and

Thus, Takasu discloses all the limitations of the claim with the exception of explicitly disclosing wherein the electrode pad extends transversely across the array of strip-shaped resistive elements; and a passivation film formed over an uppermost metal wiring layer of the semiconductor apparatus and having a window arranged to expose

the electrode pad. However, **Zuniga** teaches an analogous semiconductor apparatus wherein an electrode pad **(514/515, Figs. 5 and 6)** is formed over an array of resistive elements **(passive resistors)** such that said electrode pad **(514/515)** extends transversely across said array **(¶ [0052], Figs. 5 and 6)**. Furthermore, **Reiner** teaches an analogous semiconductor apparatus including a passivation film **(see Fig. 2 below)** former over an uppermost metal wiring layer **(metal 5)** of the semiconductor apparatus and having a window arranged to expose an electrode pad **(4).**

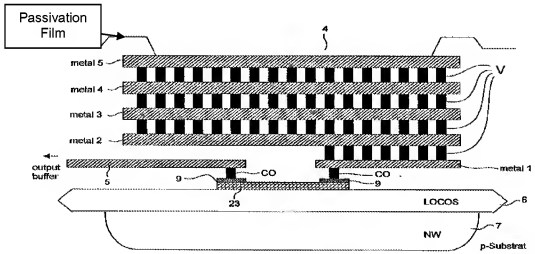


FIG.2

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to incorporate the teachings of Zuniga and Reiner, into the apparatus of Takasu, for the disclosed intended purpose of saving chip space **(Zuniga: ¶ [0049])** and improving the functionality and reliability of the device **(¶ [0036]-[0037])**.

With respect to **claim 20, Takasu** teaches wherein a respective low-resistance silicon region **(401, FIG. 1)** is formed immediately next to the lengthwise ends of each of the plurality of resistive elements **(¶ [0061])**. Note, regarding the limitation of

"polysilicon," such a material for thin film resistors is well known and conventional **(¶ [0064])**, and thus would have been obvious to one of ordinary skill in the art at the time of the invention.

7. **Claim 21** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Takasu ('177), Zuniga ('671) and Reiner ('499)** as applied to claim 19 above, and further in view of **Kohda ('313)**.

With respect to **claim 21, Takasu** further teaches wherein the oxide film **(102, Fig. 1)** comprises a MOS transistor formation region **(210)** which includes a MOS transistor comprising a gate electrode **(205)** formed of a material comprising polysilicon **(¶ [0053])**. However, Takasu does not disclose wherein the gate electrode has lengthwise ends which are bent in an upward direction over the oxide film.

However, **Khoda** teaches a semiconductor apparatus wherein the gate electrode **(4b)** has lengthwise ends which are bent in an upward direction over an oxide film **(2) (FIG. 10; col. 6, lns. 6-12)**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to incorporate the teaching of Khoda, in order to form the gate electrode with lengthwise ends bent in upward direction over an oxide film, for the disclosed intended purpose of reducing the horizontal spacing between the gates, which thereby reduces the cell area and leads to a higher cell density of memory devices **(col. 6: lns. 21-24)**.

***Response to Arguments***

8. Applicant's arguments filed December 29, 2008, have been fully considered but are moot in view of new grounds of rejection.

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abul Kalam whose telephone number is (571)272-8346.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. K./
Examiner, Art Unit 2814

/Phat X. Cao/
Primary Examiner, Art Unit 2814